



**L2012**

**LIQUID CRYSTAL DISPLAY MODULE**

**USER'S MANUAL**

## 1. GENERAL

### 1.1 General

The L2012 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

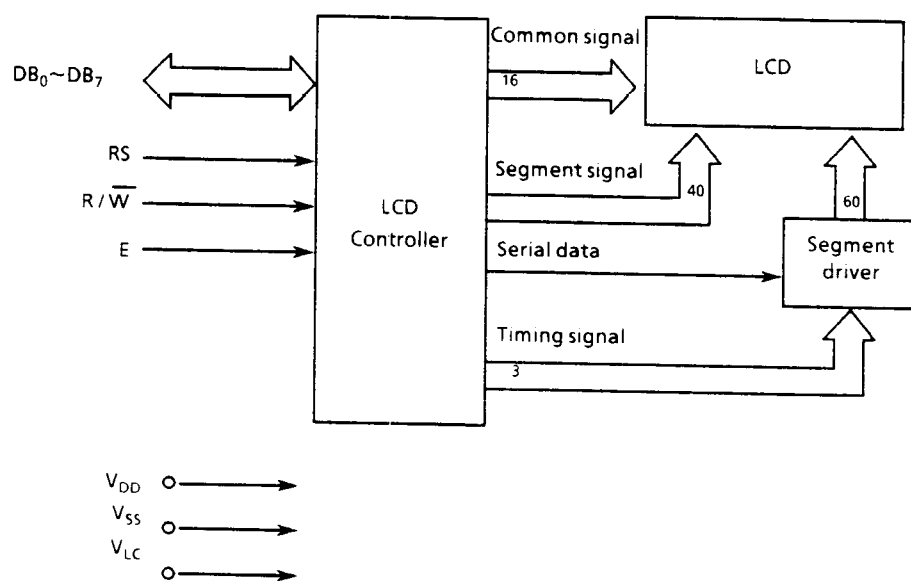
### 1.2 Features

- 20-character, two-line liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types  
(character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)  
(character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift

- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

### 1.3 Block Diagram



**Figure 1**

## 1.4 Absolute Maximum Ratings

$$V_{SS} = 0\text{ V}$$

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	$V_{DD}$	- 0.3 to + 7.0	V	
	$V_{LC}$	$V_{DD} - 7.0$ to $V_{DD} + 0.3$	V	
Input voltage	$V_{in}$	- 0.3 to $V_{DD} + 0.3$	V	
Operating temperature	$T_{opr}$	0 to + 50	°C	
Storage temperature	$T_{stg}$	- 20 to + 60	°C	At 50% RH

## 1.5 Electrical Characteristics

$$V_{DD} = 5\text{ V} \pm 5\%, \quad V_{SS} = 0\text{ V}, \quad T_a = 0^\circ\text{C to } 50^\circ\text{C}$$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage*	High	$V_{IH1}$		2.2	—	$V_{DD}$	V
	Low	$V_{IL1}$		0	—	0.6	V
Output voltage**	High	$V_{OH1}$	$-I_{OH} = 0.205\text{ mA}$	2.4	—	—	V
	Low	$V_{OL1}$	$I_{OL} = 1.2\text{ mA}$	—	—	0.4	V
Power supply voltage		$V_{DD}$		4.75	5.00	5.25	V
		$V_{DD}-V_{LC}$		3.0	—	6.0	V
Current consumption		$I_{DD}$		—	2.0	3.0	mA
		$I_{LC}$	$V_{LC} = 0.25\text{ V}$	—	0.2	1.0	mA
Clock oscillation freq.		$f_{osc}$	Resistance oscillation	190	270	350	kHz

\* Applied to  $DB_0$  to  $DB_7$ , E,  $R/\overline{W}$ , and RS

\*\* Applied to  $DB_0$  to  $DB_7$

**Remark:** Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage ( $V_{opr}$ ), that is  $V_{LC}$ .

The optical characteristics is influenced by an ambient temperature. The recommended value of  $V_{opr}$  for an ambient temperatures are shown below.

$$V_{opr} = V_{DD} - V_{LC}$$

Temperature (°C)	0	10	25	40	50
$V_{opr}$ (V)	5.00~4.80	4.90~4.70	4.75~4.60	4.60~4.30	4.50~4.10

## 1.6 Timing Characteristics

### 1.6.1 Write operation

$V_{DD} = 5.0\text{ V} \pm 5\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0^\circ\text{C to } 50^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{\text{cycE}}$	1000	–	ns
Enable pulse width	High level	$PW_{\text{EH}}$	450	–	ns
Enable rise and fall time		$t_{\text{Er}}, t_{\text{Ef}}$	–	25	ns
Setup time	$\overline{\text{RS}}, \overline{\text{R/W}} \rightarrow \text{E}$	$t_{\text{AS}}$	140	–	ns
Address hold time		$t_{\text{AH}}$	10	–	ns
Data setup time		$t_{\text{DSW}}$	195	–	ns
Data hold time		$t_{\text{H}}$	10	–	ns

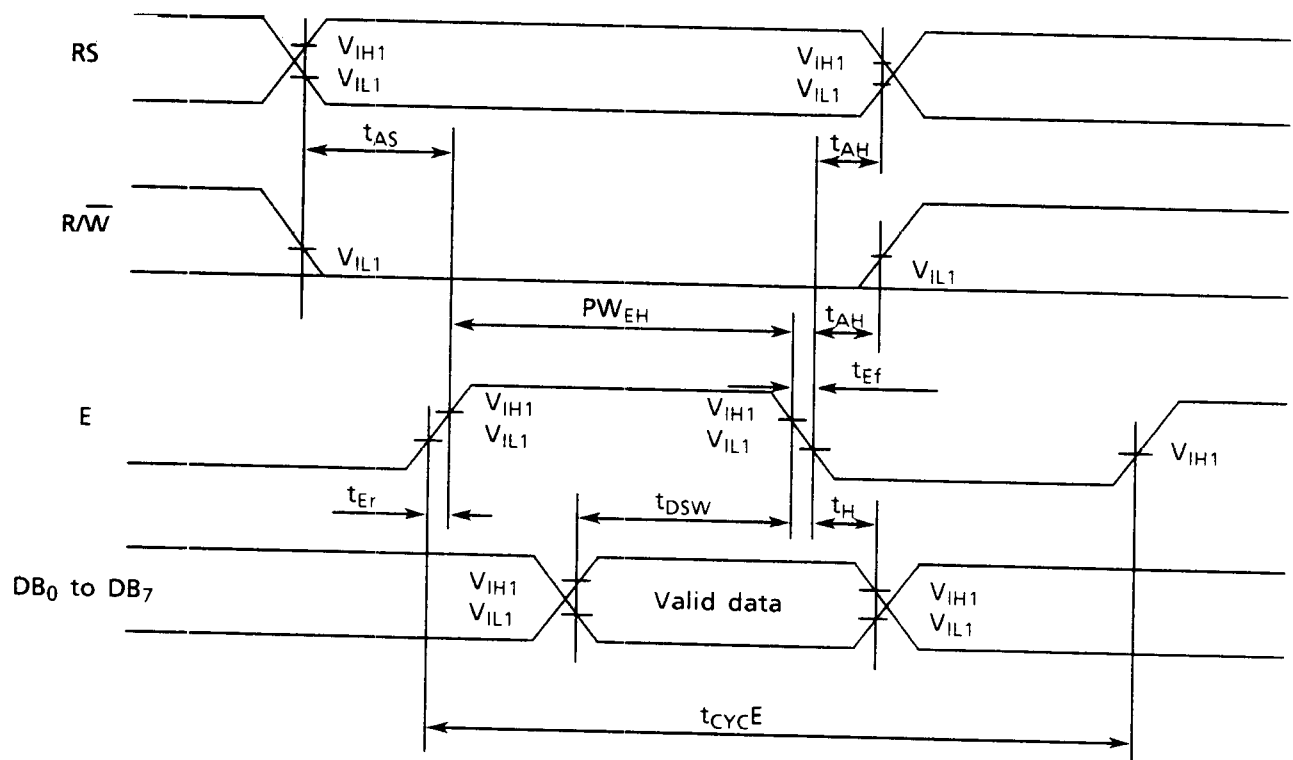


Figure 2 Data write from MPU to module

## 1.6.2 Read operation

 $V_{DD} = 5.0V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ C$  to  $50^\circ C$ 

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{CYCE}$	1000	–	ns
Enable pulse width	High level	$PW_{EH}$	450	–	ns
Enable rise and fall time		$t_{Er}, t_{Ef}$	–	25	ns
Setup time	RS, $\overline{R/W} \rightarrow E$	$t_{AS}$	140	–	ns
Address hold time		$t_{AH}$	10	–	ns
Data delay time		$t_{DDR}$	–	320	ns
Data hold time		$t_H$	20	–	ns

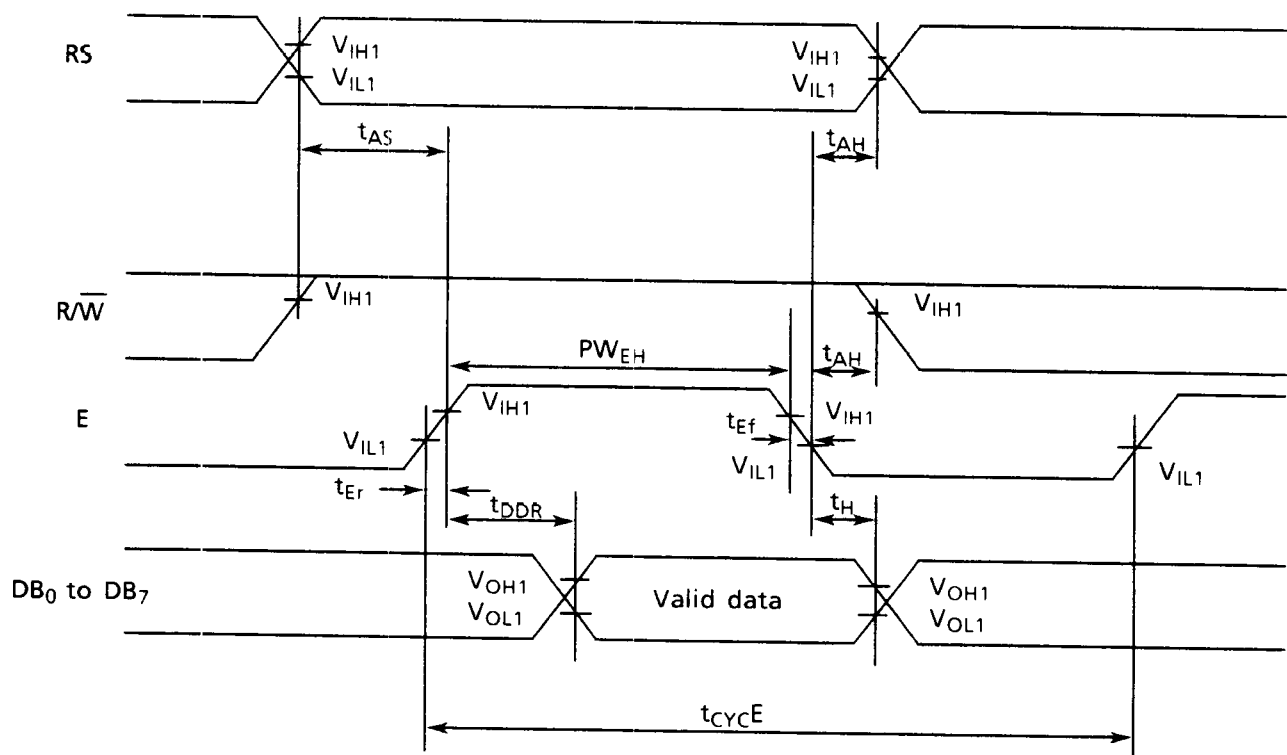


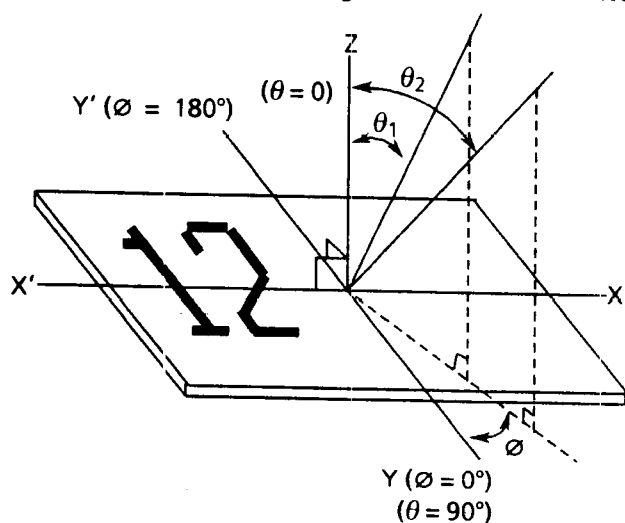
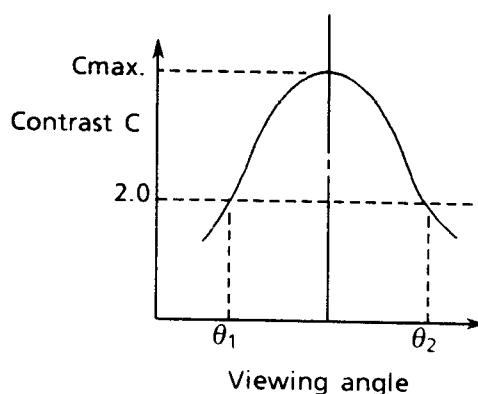
Figure 3 Data read from module to MPU

## 1.7 Optical Characteristics

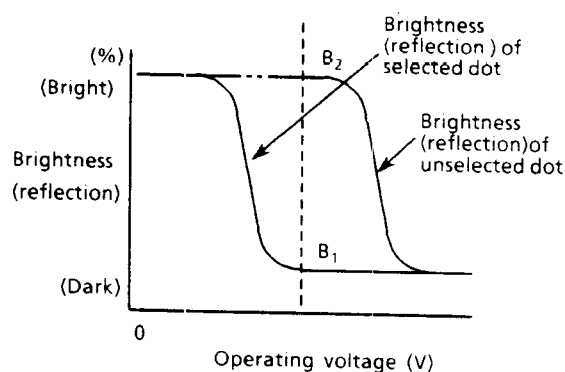
### 1.7.1 Optical characteristics (TN LCD)

Viewing angle: 6 o'clock ( $\varnothing = 0^\circ$ ) $T_a = 25^\circ\text{C}$ ,  $V_{opr} = 4.6\text{ V}$ 

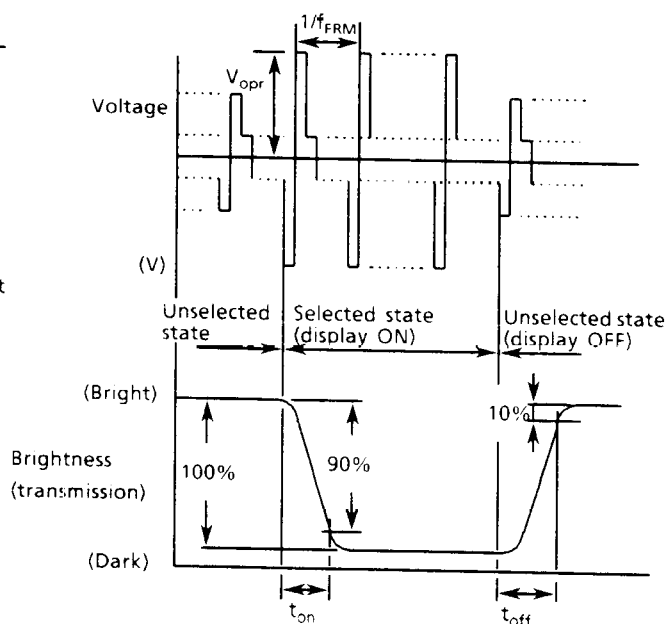
Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$ , $\varnothing = 0^\circ$	35	—	—	See Notes 1 and 2.
Contrast	$C$	$\theta = 25^\circ$ , $\varnothing = 0^\circ$	5	8	—	See Note 3.
Response time (rise)	$t_{on}$	$\theta = 25^\circ$ , $\varnothing = 0^\circ$	—	40 ms	80 ms	See Note 4.
Response time (fall)	$t_{off}$	$\theta = 25^\circ$ , $\varnothing = 0^\circ$	—	120 ms	160 ms	See Note 4.

Note 1: Definition of angles  $\varnothing$  and  $\theta$ Note 2: Definition of viewing angles  $\theta_1$  and  $\theta_2$ Note 3: Definition of contrast  $C$ 

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

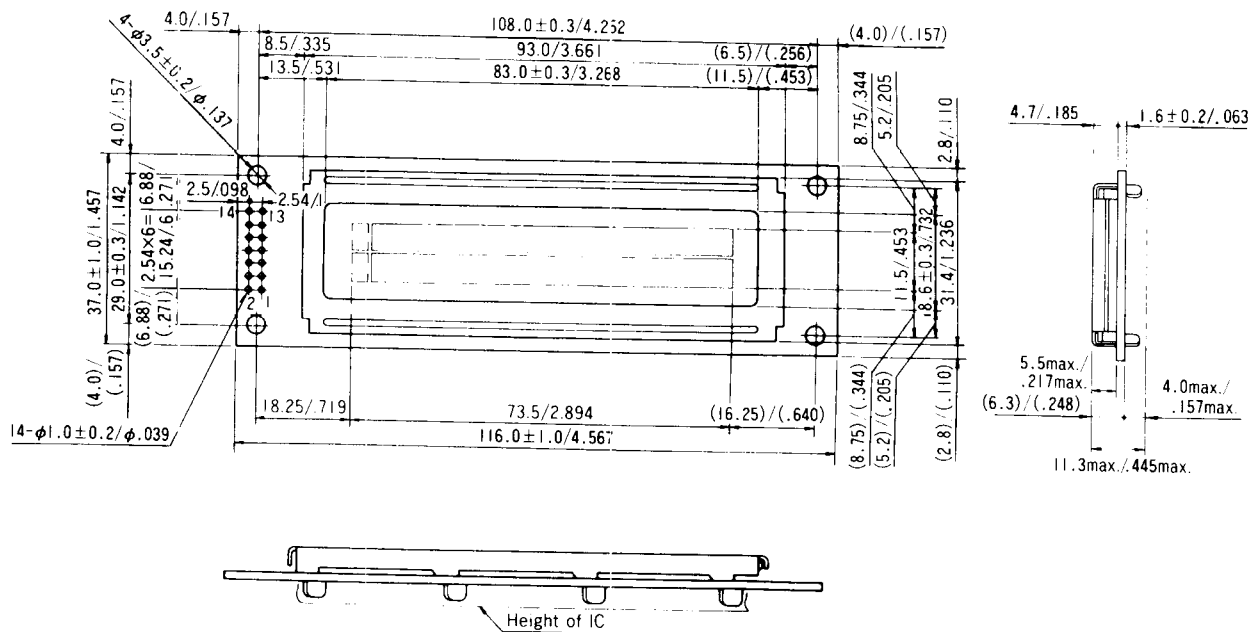


Note 4: Definition of response time

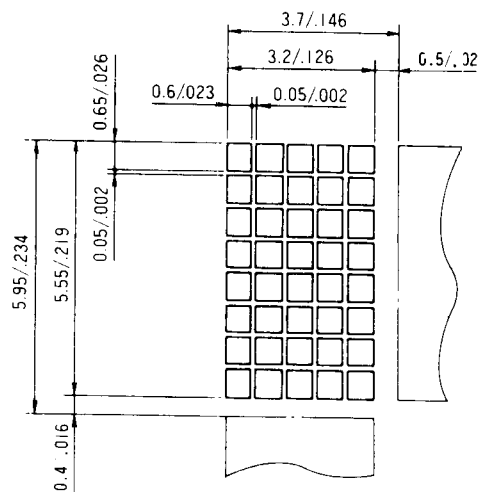


$V_{opr}$ : Operating voltage  
 $f_{FRM}$ : Frame frequency  
 $t_{on}$ : Response time (rise)  
 $t_{off}$ : Response time (fall)

## 1.8 Dimensions



Unit : mm/inch  
General tolerance :  $\pm 0.5$  mm



I/O terminal symbol

No.	Symbol
1	V <sub>SS</sub>
2	V <sub>DD</sub>
3	V <sub>LC</sub>
4	R <sub>S</sub>
5	R/W
6	E
7	DB <sub>0</sub>
8	DB <sub>1</sub>
9	DB <sub>2</sub>
10	DB <sub>3</sub>
11	DB <sub>4</sub>
12	DB <sub>5</sub>
13	DB <sub>6</sub>
14	DB <sub>7</sub>

Figure 4



## 2. OPERATING INSTRUCTIONS

### 2.1 Terminal Functions

**Table 1 Terminal functions**

Signal name	No. of terminals	I/O	Destination	Function
DB <sub>0</sub> to DB <sub>3</sub>	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB <sub>4</sub> to DB <sub>7</sub>	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB <sub>7</sub> is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/ $\overline{W}$	1	Input	MPU	Read (R) and Write ( $\overline{W}$ ) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V <sub>LC</sub>	1	--	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V <sub>LC</sub> .
V <sub>DD</sub>	1	--	Power supply	+ 5 V
V <sub>SS</sub>	1	--	Power supply	Ground terminal: 0 V

## 2.2 Basic Operations

### 2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

**Table 2 Register selection**

RS	R/W	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB <sub>7</sub> ) and address counter (DB <sub>0</sub> to DB <sub>6</sub> ) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

### 2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB<sub>7</sub> if RS = 0 and R/W = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

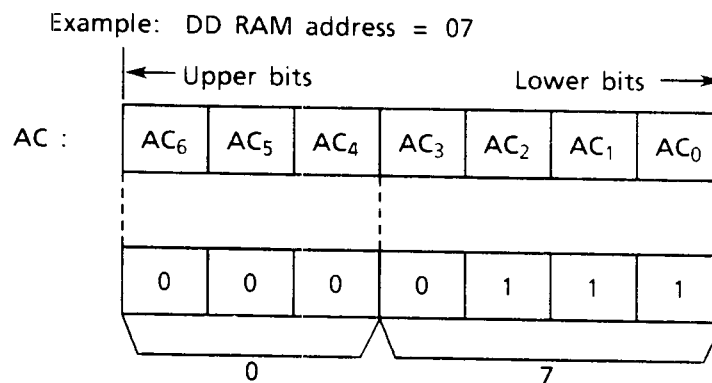
### 2.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB<sub>0</sub> to DB<sub>6</sub> as shown in Table 2 if RS = 0 and  $\overline{R/W} = 1$ .

### 2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to  $80 \times 8$  bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.



DD RAM addresses 00<sub>H</sub> to 13<sub>H</sub> are set in the line 1, and 40<sub>H</sub> to 53<sub>H</sub> in the line 2.

Note : The addresses in the digit 20 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8		13	14	15	16	17	18	19	20	Display digit
Line 1	00	01	02	03	04	05	06	07	---	0C	0D	0E	0F	10	11	12	13	DD RAM address
Line 2	40	41	42	43	44	45	46	47	---	4C	4D	4E	4F	50	51	52	53	

If the display is shifted, DD RAM addresses 00<sub>H</sub> to 27<sub>H</sub> are displayed in line 1 and 40<sub>H</sub> to 67<sub>H</sub> in line 2. The following figures are examples of display shifts.

\*Left shift

	1	2	3	4	5	6	7	8		13	14	15	16	17	18	19	20	Display digit
Line 1	01	02	03	04	05	06	07	08	---	0D	0E	0F	10	11	12	13	14	DD RAM address
Line 2	41	42	43	44	45	46	47	48	---	4D	4E	4F	50	51	52	53	54	

\*Right shift

	1	2	3	4	5	6	7	8		13	14	15	16	17	18	19	20	Display digit
Line 1	27	00	01	02	03	04	05	06	---	0B	0C	0D	0E	0F	10	11	12	DD RAM address
Line 2	67	40	41	42	43	44	45	46	---	4B	4C	4D	4E	4F	50	51	52	

### 2.2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

### 2.2.6 Character generator RAM (CG RAM)

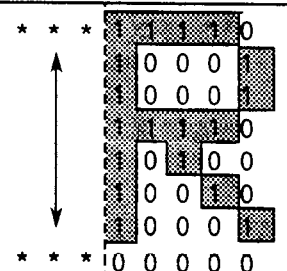
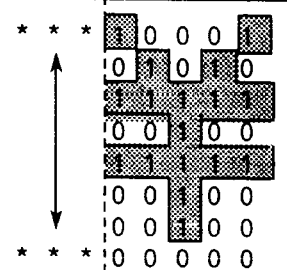
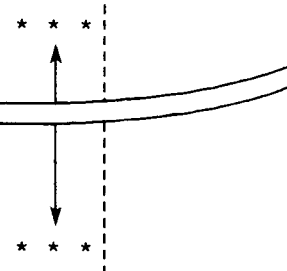
CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

**Table 3 Correspondence between character codes and character patterns**

Upper 4 bits Lower 4 bits		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
× × × × 0000	CG RAM (1)			0	a	P	`	P		—	9	3	0	P
	(2)	!	1	A	O	a	9	3	7	7	4	3	a	a
× × × × 0010	(3)	"	2	B	R	b	r	r	4	4	7	P	B	B
	(4)	#	3	C	S	c	s	4	9	7	3	e	e	e
× × × × 0100	(5)	*	4	D	T	d	t	`	I	t	+	u	a	a
	(6)	%	5	E	U	e	u	3	*	*	1	e	U	U
× × × × 0101	(6)	%	5	E	U	e	u	3	*	*	1	e	U	U
	(7)	8	6	F	V	f	v	9	h	2	3	a	Σ	Σ
× × × × 0110	(7)	8	6	F	V	f	v	9	h	2	3	a	Σ	Σ
	(8)	'	7	G	W	g	w	7	+	7	9	a	π	π
× × × × 1000	(1)	<	8	H	X	h	x	4	9	*	1	7	Σ	Σ
	(2)	)	9	I	V	i	w	3	7	1	3	7	u	u
× × × × 1010	(3)	*	3	J	Z	j	z	3	3	h	1	i	7	7
	(4)	+	3	K	E	k	4	*	9	7	0	*	7	7
× × × × 1011	(4)	+	3	K	E	k	4	*	9	7	0	*	7	7
	(5)	:	<	L	*	1	1	+	3	7	7	9	7	7
× × × × 1101	(6)	—	=	M	1	m	)	3	7	3	0	4	+	+
	(7)	:	>	N	^	n	+	3	7	+	3	h		
× × × × 1111	(8)	/	?	O	—	o	+	3	7	7	3	0	7	7

**Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)**

Character code (DD RAM data)	CG RAM address	Character pattern (CG RAM data)
7 6 5 4 3 2 1 0 ← Upper bit Lower bit →	5 4 3 2 1 0 ← Upper bit Lower bit →	7 6 5 4 3 2 1 0 ← Upper bit Lower bit →
0 0 0 0 * 0 0 0	0 0 0	 <p>Example of character pattern (R)</p> <p>← Cursor position</p>
0 0 0 0 * 0 0 1	0 0 1	 <p>Example of character pattern (Y)</p>
0 0 0 0 * 1 1 1	1 1 1	

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.
- The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00H and 08H select the same character.

## 2.3 Instruction Outline

**Table 5 List of instructions**

Instruction	Code											Function	Execution time#
	RS	R/W	DB <sub>7</sub>	DB <sub>6</sub>	DB <sub>5</sub>	DB <sub>4</sub>	DB <sub>3</sub>	DB <sub>2</sub>	DB <sub>1</sub>	DB <sub>0</sub>			
(1) Display clear	0	0	0	0	0	0	0	0	0	1		Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*		Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S		Sets direction of cursor movement and whether display will be shifted when data is written or read	40 $\mu$ s
(4) Display ON/OFF control	0	0	0	0	0	0	1	D	C	B		Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 $\mu$ s
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*		Moves cursor and shifts display without changing DD RAM contents	40 $\mu$ s
(6) Function Set	0	0	0	0	1	DL	N	F	*	*		Sets interface data length (DL), the number of display lines (N), and character fonts (F)	40 $\mu$ s
(7) CG RAM Address Set	0	0	0	1	A <sub>CG</sub>							Sets CG RAM address to start transmitting or receiving CG RAM data	40 $\mu$ s
(8) DD RAM Address Set	0	0	1	A <sub>DD</sub>								Sets DD RAM address to start transmitting or receiving DD RAM data	40 $\mu$ s
(9) BF/Address Read	0	1	BF	AC								Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 $\mu$ s
(10) Data Write to CG RAM or DD RAM	1	0	Write Data									Writes data into DD RAM or CG RAM	40 $\mu$ s
(11) Data Read from CG RAM or DD RAM	1	1	Read Data									Reads data from DD RAM or CG RAM	40 $\mu$ s

\* : Invalid bit

A<sub>CG</sub> : CG RAM address

A<sub>DD</sub> : DD RAM address

AC : Address counter

I/D = 1 : Increment

I/D = 0 : Decrement

B = 1 : Blink ON

B = 0 : Blink OFF

N = 1 : 2 lines

N = 0 : 1 line

S = 1 : Display shift

S = 0 : No display shift

S/C = 1 : Display shift

S/C = 0 : Cursor movement

F = 1 : 5 × 10 dot matrix

F = 0 : 5 × 7 dot matrix

D = 1 : Display ON

D = 0 : Display OFF

R/L = 1 : Right shift

R/L = 0 : Left shift

BF = 1 : Internal operation in progress

BF = 0 : Instruction can be accepted

C = 1 : Cursor ON

C = 0 : Cursor OFF

DL = 1 : 8 bits

DL = 0 : 4 bits

# An execution time indicates maximum value when  $f_{osc}$  is 250 kHz. It changes at the inverse proportion of  $f_{osc}$ .

## 2.4 Instruction Details

### (1) Display Clear

	RS	R/W	DB <sub>7</sub>						DB <sub>0</sub>
Code	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

### (2) Cursor Home

	RS	R/W	DB <sub>7</sub>						DB <sub>0</sub>
Code	0	0	0	0	0	0	0	1	*

\* : Don't care bit

Cursor Home returns cursor to home position (address 0). DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

**Table 6 Restrictions on execution of Display Clear and Cursor Home instructions**

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$ second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for $f_{osc} = 270$ kHz * $f_{osc}$ : Oscillation frequency
When 23 <sub>H</sub> , 27 <sub>H</sub> , 63 <sub>H</sub> , or 67 <sub>H</sub> is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)



## (3) Entry Mode Set

	RS	R/W	DB <sub>7</sub>						DB <sub>0</sub>	
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.

When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

## (4) Display ON/OFF Control

	RS	R/W	DB <sub>7</sub>						DB <sub>0</sub>	
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.

When D = 0, the display is turned OFF.

If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

**C :** When C = 1, the cursor is displayed.

When C = 0, the cursor is not displayed.

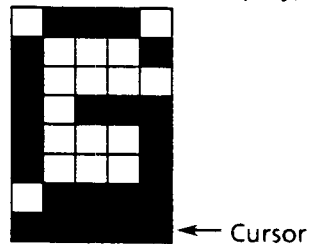
The cursor is displayed in the dot line below the character fonts.

**B :** When B = 1, the character at the cursor position starts blinking.

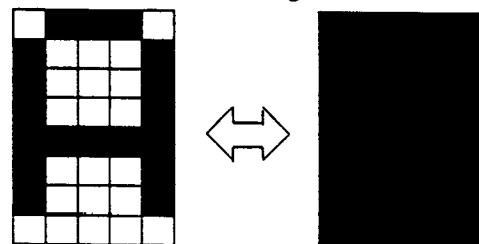
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds when  $f_{osc}$  is 250 kHz. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display)



B = 1 (blinking)



#### (5) Cursor/Display Shift

	RS	R/W	DB <sub>7</sub>							DB <sub>0</sub>	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* : Don't care bit

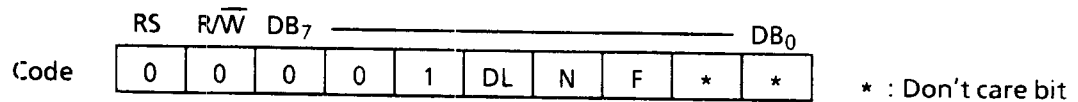
Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character by two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Note: If only display shift is done, the AC contents do not change.

## (6) Function Set



Function Set sets the interface data length, the number of display lines, and the character font.

**DL :** Interface data length

When DL = 1, the data length is set at eight bits (DB<sub>7</sub> to DB<sub>0</sub>).

When DL = 0, the data length is set at four bits (DB<sub>7</sub> to DB<sub>4</sub>).

The upper four bits are transferred first, then the lower four bits follow.

**N :** Number of display lines

When N = 1, the display line is set to two lines.

When N = 0, the display line is set to one line.

For L2012, set N to 1.

**F :** Character font

When F = 1, the character font is set to 5×10 dot matrix.

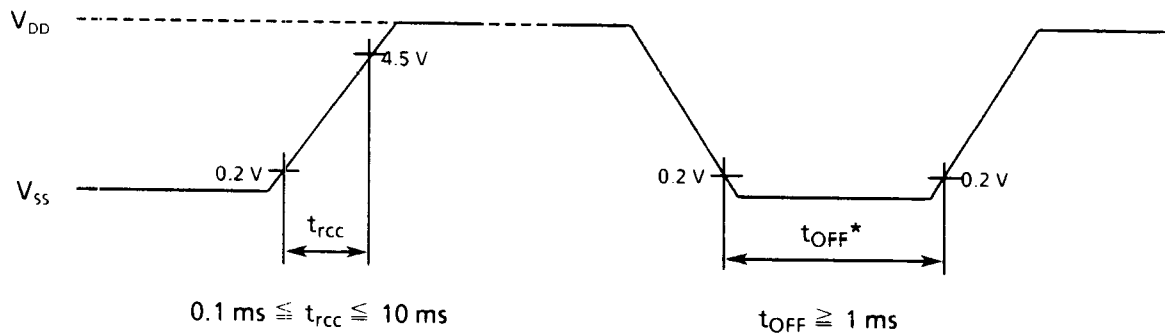
When F = 0, the character font is set to 5×7 dot matrix.

If N is set to 1, F becomes "Don't care bit". For L2012, set F to 0 or 1.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

**Remarks: Initialization****1. Automatic initialization**

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



\* $t_{OFF}$ : Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

The following instructions are executed for initialization.

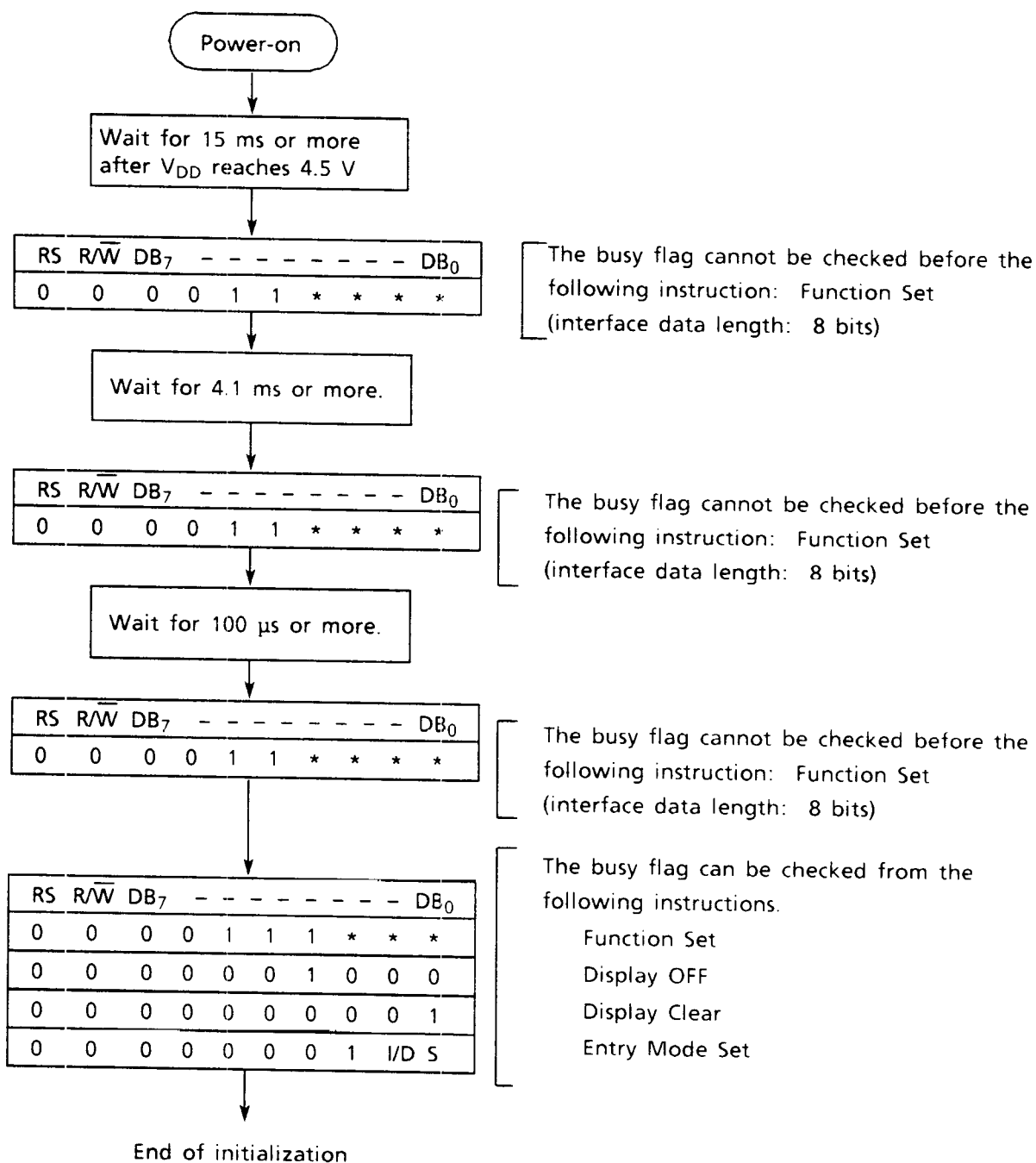
- Display Clear
- Function Set
  - DL = 1: Interface data length: Eight bits
  - N=0: One line display
  - F=0: Character font: 5×7 dot matrix
- Display ON/OFF Control
  - D = 0: Display OFF
  - C = 0: Cursor OFF
  - B = 0: Blink OFF
- Entry Mode Set
  - I/O = 1: Increment
  - S = 0: No display shift

Since the condition is not suitable for the L2012, further Function Set instruction is necessary.

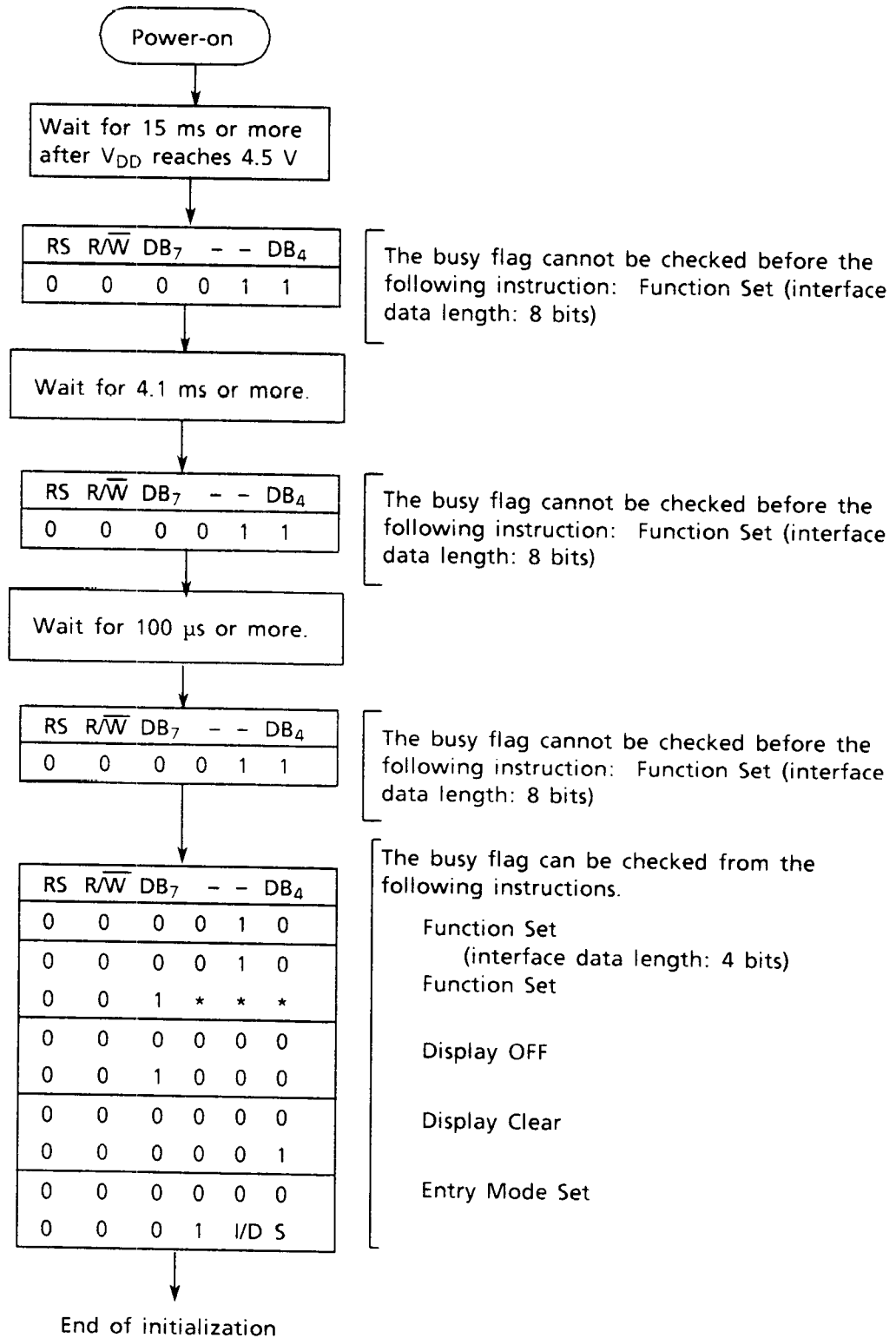
## 2. Initialization by instructions

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the following instructions. Since it is unknown whether the interface data length is set to eight bits or four bits at power on, execute Function Set twice to set the interface data length to eight bits. And then for setting the required interface data length execute further Function Set instruction.

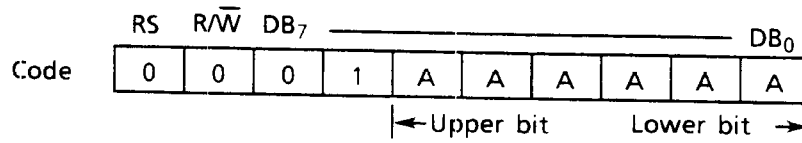
### (a) Interface data length : Eight bits



## (b) Interface data length: Four bits

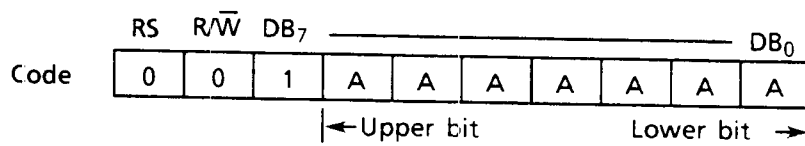


## (7) CG RAM Address Set



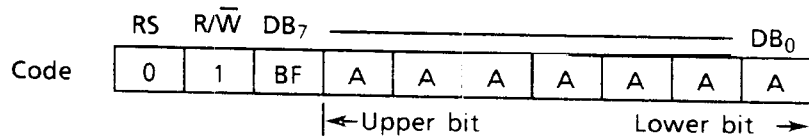
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

## (8) DD RAM Address Set



DD RAM addresses expressed as binary AAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAA) are 00H to 27H and those for line 2 (AAAAAA) are 40H to 67H.

## (9) Busy Flag/Address Read



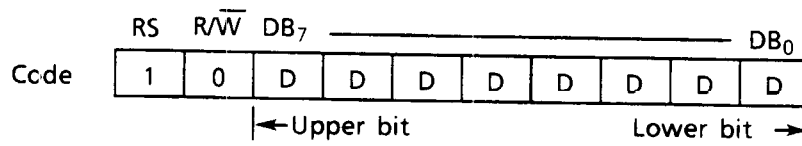
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

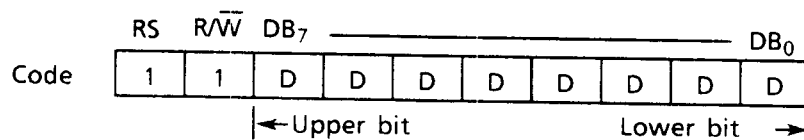
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

## (10) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

## (11) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

**Note :** The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.



## 2.5 Examples of Instruction Use

### 2.5.1 Interface data length: Eight bits

No.	Instruction	Display	Operation						
1	Power-on <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td></td><td></td><td></td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>					The built-in reset circuit initializes the module.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
2	Function Set <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>0 0 1 1 1 * * *</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	0	0	0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
0	0	0 0 1 1 1 * * *							
3	Display ON/OFF Control <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 1 1 1 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	0	0	0 0 0 0 1 1 1 0		The display and cursor are turned ON, but nothing is displayed.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
0	0	0 0 0 0 1 1 1 0							
4	Entry Mode Set <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 1 1 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	0	0	0 0 0 0 0 1 1 0		The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
0	0	0 0 0 0 0 1 1 0							
5	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 1 0 0 1 1 0 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	1	0	0 1 0 0 1 1 0 0		L is written. The AC is incremented by one and the cursor shifts to the right.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
1	0	0 1 0 0 1 1 0 0							
6	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 1 0 0 0 0 1 1</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	1	0	0 1 0 0 0 0 1 1		C is written.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
1	0	0 1 0 0 0 0 1 1							
7									
8	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub> — DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 0 1 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>	1	0	0 0 1 1 0 0 1 0		2 is written in digit 20. Cursor disappears.
RS	R/W	DB <sub>7</sub> — DB <sub>0</sub>							
1	0	0 0 1 1 0 0 1 0							

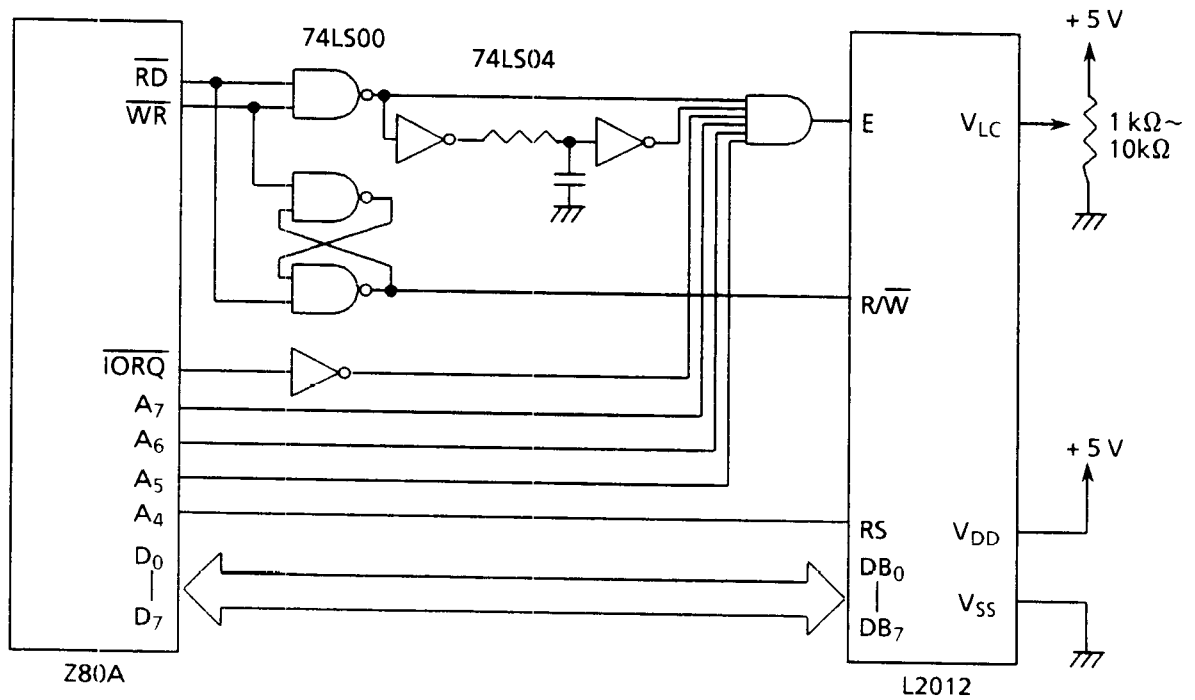
No.	Instruction	Display	Operation														
9	DD RAM address set <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>1 1 0 0 0 0 0 0</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	0	0	1 1 0 0 0 0 0 0		<table><tr><td>LCD</td><td>-----</td><td>L2012</td></tr><tr><td colspan="3">_</td></tr></table>	LCD	-----	L2012	_			The DD RAM address is set so that the cursor appears at digit 1 of line 2.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
0	0	1 1 0 0 0 0 0 0															
LCD	-----	L2012															
_																	
10	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 0 1 0</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	1	0	0 0 1 1 0 0 1 0		<table><tr><td>LCD</td><td>-----</td><td>L2012</td></tr><tr><td colspan="3">2_</td></tr></table>	LCD	-----	L2012	2_			2 is written.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
1	0	0 0 1 1 0 0 1 0															
LCD	-----	L2012															
2_																	
11	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 0 0 0</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	1	0	0 0 1 1 0 0 0 0		<table><tr><td>LCD</td><td>-----</td><td>L2012</td></tr><tr><td colspan="3">20_</td></tr></table>	LCD	-----	L2012	20_			0 is written.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
1	0	0 0 1 1 0 0 0 0															
LCD	-----	L2012															
20_																	
12																	
13	Write to CG RAM or DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>1</td><td>0</td><td>0 1 0 1 0 0 1 1</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	1	0	0 1 0 1 0 0 1 1		<table><tr><td>LCD</td><td>-----</td><td>L2012</td></tr><tr><td colspan="3">20 ----- 2 LINES</td></tr></table>	LCD	-----	L2012	20 ----- 2 LINES			5 is written.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
1	0	0 1 0 1 0 0 1 1															
LCD	-----	L2012															
20 ----- 2 LINES																	
14	DD RAM address set <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>1 0 0 0 0 0 0 0</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	0	0	1 0 0 0 0 0 0 0		<table><tr><td>LCD</td><td>-----</td><td>L2012</td></tr><tr><td colspan="3">20 ----- 2 LINES</td></tr></table>	LCD	-----	L2012	20 ----- 2 LINES			The cursor returns to the home position.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
0	0	1 0 0 0 0 0 0 0															
LCD	-----	L2012															
20 ----- 2 LINES																	
15	Display clear <table><tr><td>RS</td><td>R/W</td><td>DB<sub>7</sub></td><td>DB<sub>0</sub></td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 0 0 1</td><td></td></tr></table>	RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>	0	0	0 0 0 0 0 0 0 1		<table><tr><td colspan="3">_</td></tr><tr><td colspan="3"></td></tr></table>	_						All the display disappears and the cursor remains at the home position.
RS	R/W	DB <sub>7</sub>	DB <sub>0</sub>														
0	0	0 0 0 0 0 0 0 1															
_																	
16																	

## 2.5.2 Interface data length: Four bits

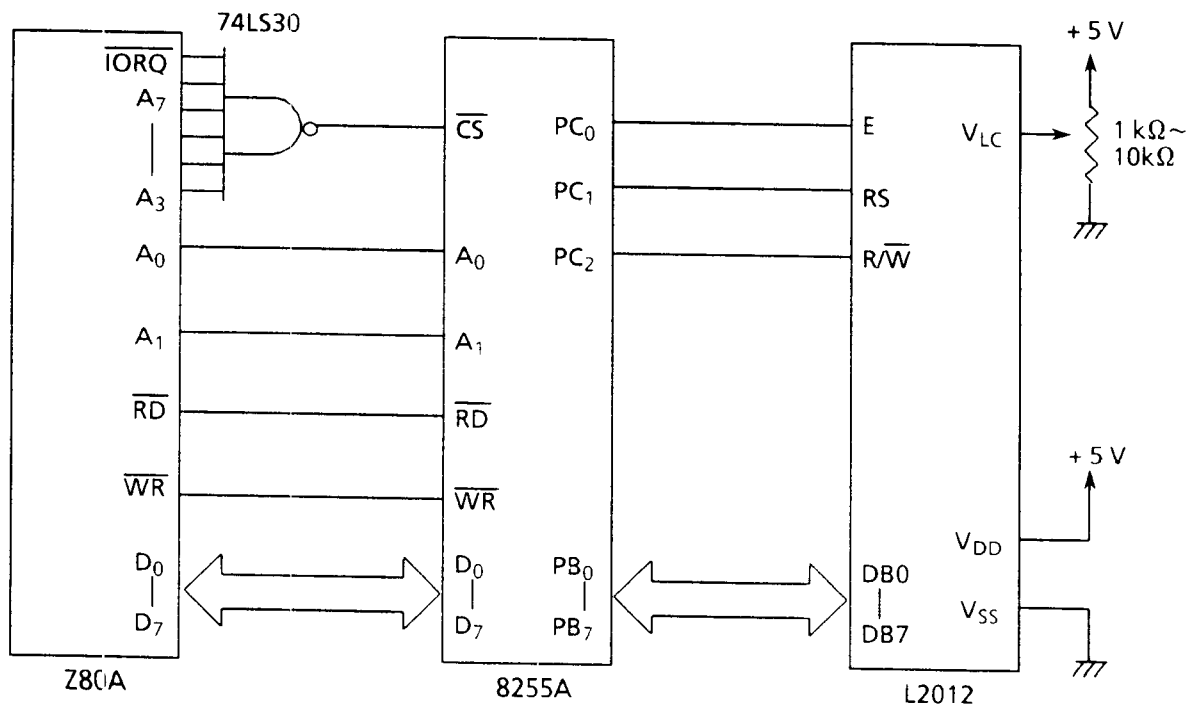
No.	Instruction	Display	Operation											
1	<p>Power-on</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td></td><td></td><td></td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>				<table><tr><td></td></tr><tr><td></td></tr></table>			The built-in reset circuit initializes the module.			
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
2	<p>Function Set</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td>0</td><td>0</td><td>0 0 1 0</td></tr><tr><td></td><td></td><td></td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>	0	0	0 0 1 0				<table><tr><td></td></tr><tr><td></td></tr></table>			Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
0	0	0 0 1 0												
3	<p>Function Set</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td>0</td><td>0</td><td>0 0 1 0</td></tr><tr><td>0</td><td>0</td><td>1 * * *</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>	0	0	0 0 1 0	0	0	1 * * *	<table><tr><td></td></tr><tr><td></td></tr></table>			The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
0	0	0 0 1 0												
0	0	1 * * *												
4	<p>Display ON/OFF Control</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td></tr><tr><td>0</td><td>0</td><td>1 1 1 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>	0	0	0 0 0 0	0	0	1 1 1 0	<table><tr><td>_</td></tr><tr><td></td></tr></table>	_		The display and cursor are turned ON, but nothing is displayed.
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
0	0	0 0 0 0												
0	0	1 1 1 0												
_														
5	<p>Entry Mode Set</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td></tr><tr><td>0</td><td>0</td><td>0 1 1 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>	0	0	0 0 0 0	0	0	0 1 1 0	<table><tr><td>_</td></tr><tr><td></td></tr></table>	_		The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
0	0	0 0 0 0												
0	0	0 1 1 0												
_														
6	<p>Write to CG RAM or DD RAM</p> <table><tr><th>RS</th><th>R/W</th><th>DB<sub>7</sub> — DB<sub>4</sub></th></tr><tr><td>1</td><td>0</td><td>0 1 0 0</td></tr><tr><td>1</td><td>0</td><td>1 1 0 0</td></tr></table>	RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>	1	0	0 1 0 0	1	0	1 1 0 0	<table><tr><td>L _</td></tr><tr><td></td></tr></table>	L _		L is written. the AC is incremented by one and the cursor shifts to the right.
RS	R/W	DB <sub>7</sub> — DB <sub>4</sub>												
1	0	0 1 0 0												
1	0	1 1 0 0												
L _														
7														

## 2.6 MPU Connection Diagrams

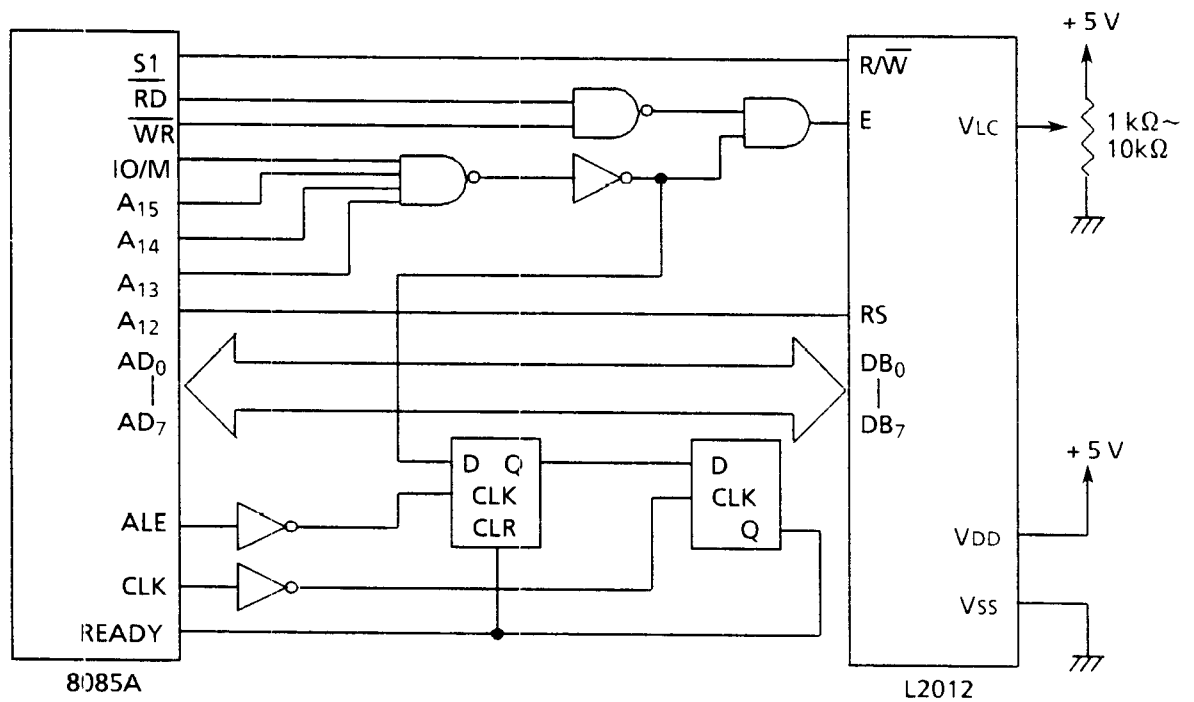
### 2.6.1 Z80A



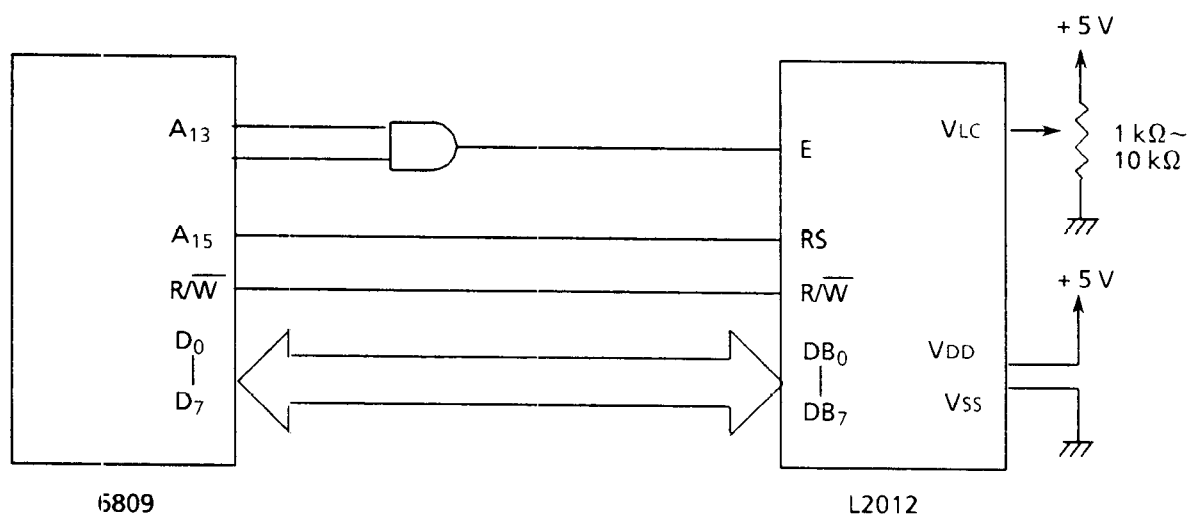
### 2.6.2 Z80A and 8255A



## 2.6.3 8085A



## 2.6.4 6809



### 3. NOTES

#### Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

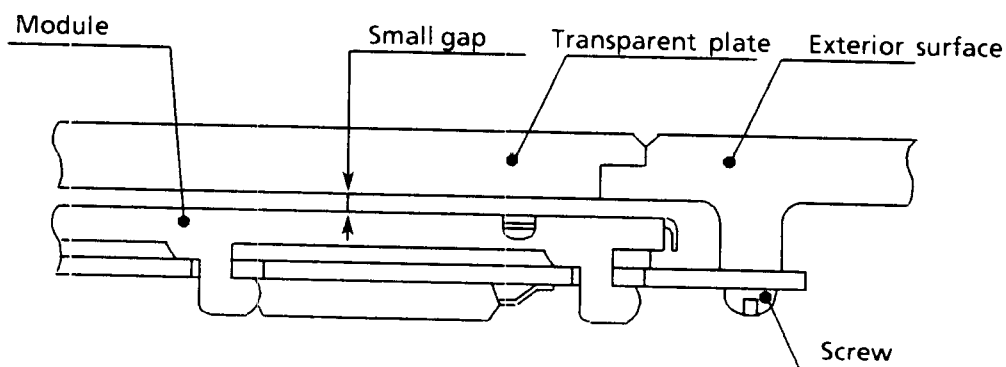
#### Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile; handle it very carefully.

#### Mounting and esign

- Mount the module by using the specified mounting part and holes.
- Connect a 10- $\mu$ F capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plates (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizer.

#### ☆ Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

**Storage**

- Store the module in a dark place where the temperature is  $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$  and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

**Cleaning**

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.